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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/018,179	Examiner:	Pham, Hoai V.
Confirmation No.:	8545	Art Unit:	2814
Filing Date:	May 3, 2002	Atty. Dkt. No:	5310-03900
Inventor(s):	Skotnicki et al.		
Title:	SEMICONDUCTOR DEVICE WITH COMPENSATED THRESHOLD VOLTAGE AND METHOD FOR MAKING SAME		

CERTIFICATE OF MAILING
UNDER 37 C.F.R. §1.8

DATE OF DEPOSIT: 6-11-03

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Jackie L. Pitre

RESPONSE TO OFFICE ACTION MAILED FEBRUARY 12, 2003

Mail Stop Non-Fee Amendment
Commissioner for Patents
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Alexandria, VA 22313-1450

A. Pending Claims

Claims 9-28 are currently pending.

B. The Claims Are Definite Pursuant To 35 U.S.C. § 112, First Paragraph

The Examiner rejected claims 21 and 22 under 35 U.S.C. § 112, first paragraph, as "containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to

make and/or use the invention." Applicant respectfully disagrees.

The Examiner states: " 'the set of conditions comprises an implantation angle of incidence with respect to the normal angle to the substrate, an implantation dose, and an implantation energy' is not described in the specification and shown in the figures."

Applicant submits that the features of claims 21 and 22 including "wherein the set of conditions comprises an implantation angle of incidence with respect to the normal angle to the substrate, an implantation dose, and an implantation energy" are described in the Specification (Substitute Sheets) at least on page 5, lines 8-19 which states:

> As is known, the formation of doped pockets in a semiconductor substrate depends on the angle of incidence of the implantation with respect to the normal to the substrate, on the implantation dose, and on the implantation energy of the dopant. Thus, by varying the angle of incidence and the dopant dose, it is possible to increase the length of the implanted pocket and to vary the dopant concentration.
>
> As a variant, in order to vary the length of the second implanted pockets and their dopant concentration, successive implantation steps may be carried out with the same angle of incidence with respect to the normal, the same dose, and the same implantation energy. However, subjecting the device to a different annealing heat treatment step after each successive implantation step may make the dopant implanted in the substrate diffuse differently for each implanted pocket. (Specification, Substitute Sheet, page 5, lines 8-19)

C. The Claims Are Not Anticipated By Hshieh Pursuant To 35 U.S.C. § 102(b)

The Examiner rejected claims 9, 10, 12-16 and 23-28 under 35 U.S.C. 103(a) as anticipated by U.S. Patent No. 5,731,611 to Hshieh et al. (hereinafter "Hshieh"). Applicant respectfully disagrees with the rejections.

The standard for "anticipation" is one of fairly strict identity. To anticipate a claim of a patent, a single prior source must contain all the claimed essential elements. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 U.S.P.Q.81, 91 (Fed. Cir. 1986); *In re*

Donahue, 766 F.2d 531,226 U.S.P.Q. 619,621 (Fed. Cir. 1985).

The Examiner states:

With respect to claim 9, Hshieh (figs. 6A-6D, cols. 5-6) discloses a semiconductor device, comprising:

a semiconductor substrate (210) having a predetermined concentration, Ns, of a dopant of a first conductivity type;

a source region (265) and a drain region (265) doped with a dopant of a second conductivity type;

junctions, wherein the junctions delimit a channel region of a predetermined length, L_N in the substrate, wherein the junctions are defined by the source region and the drain region;

first pockets (250) located adjacent to each of the junctions, wherein the pockets have a predetermined length, Lp, wherein the first pockets are doped with a dopant of the first conductivity type with a dopant concentration, Np, which locally increases a net concentration in the substrate above Ns;

second pockets (230) located adjacent to each of the junctions and stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, and wherein the second pockets are doped with a dopant of the second conductivity type with a dopant concentration, Nn, such that Nn is less than Np, which locally decreases a net concentration without changing a conductivity type, and wherein Nn is less than Ns; and

wherein an overall length of the first pockets and the second pockets is less than the length, LN, of the channel region (fig. 6D).

The Examiner further states:

With respect to claim 16, Hshieh (figs. 6A-6D, cols. 5-6) discloses a method for fabricating a semiconductor device, comprising:

forming a semiconductor substrate (210) with a predetermined concentration, Ns, of a dopant of a first conductivity type;

forming a source region (265) and a drain region (265) by doping the source and drain regions with a dopant of a second conductivity type, wherein the second conductivity type is opposite the first conductivity type, wherein the source and drain regions form junctions that delimit a channel region between them, and wherein the channel region comprises a predetermined length, L_N;

forming first pockets (250) adjacent to each of the junctions in the channel region, wherein first pockets are formed by doping each of the first pockets with a predetermined concentration, Np, of a dopant of the first conductivity type, which locally increases a net concentration in the substrate

above Ns, and wherein each of the first pockets comprises a predetermined length, Lp; and

implanting in the channel region a dopant of the second conductivity type under a set of conditions such that second pockets (230) are formed in the channel region, where the second pockets are stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, wherein the second pockets have a concentration, Nn, of the dopant of the second conductivity type such that Nn is less than Np, which locally decreases a net concentration without changing a conductivity type, wherein Nn is less than Ns, and wherein the overall length of the first pockets and the second pockets is less than the nominal length, LN, of the channel region.

Claim 9 describes a combination of features including:

a semiconductor substrate having a predetermined concentration, Ns, of a dopant of a first conductivity type;

a source region and a drain region doped with a dopant of a second conductivity type;

junctions, wherein the junctions delimit a channel region of a predetermined length, L_N, in the substrate, wherein the junctions are defined by the source region and the drain region;

first pockets located adjacent to each of the junctions, wherein the pockets have a predetermined length, Lp, wherein the first pockets are doped with a dopant of the first conductivity type with a dopant concentration, Np, which locally increases a net concentration in the substrate above Ns;

second pockets located adjacent to each of the junctions and stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, and wherein the second pockets are doped with a dopant of the second conductivity type with a dopant concentration, Nn, such that Nn is less than Np, which locally decreases a net concentration without changing a conductivity type, and wherein Nn is less than Ns; and

wherein an overall length of the first pockets and the second pockets is less than the length, L_N, of the channel region.

Claim 16 describes a combination of features including:

forming a semiconductor substrate with a predetermined concentration, Ns, of a dopant of a first conductivity type;

> forming a source region and a drain region by doping the source and drain regions with a dopant of a second conductivity type, wherein the second conductivity type is opposite the first conductivity type, wherein the source and drain regions form junctions that delimit a channel region between them, and wherein the channel region comprises a predetermined length, L_N;
>
> forming first pockets adjacent to each of the junctions in the channel region, wherein the first pockets are formed by doping each of the first pockets with a predetermined concentration, Np, of a dopant of the first conductivity type, which locally increases a net concentration in the substrate above Ns, and wherein each of the first pockets comprises a predetermined length, Lp; and
>
> implanting in the channel region a dopant of the second conductivity type under a set of conditions such that second pockets are formed in the channel region, wherein the second pockets are stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, wherein the second pockets have a concentration, Nn, of the dopant of the second conductivity type such that Nn is less than Np, which locally decreases a net concentration without changing a conductivity type, wherein Nn is less than Ns, and wherein the overall length of the first pockets and the second pockets is less than the nominal length, L_N, of the channel region.

The device of Hshieh is directed toward a vertical diffused semiconductor device. Furthermore, Hshieh appears to teach a semiconductor device with a drain region doped with impurities of a first conductivity type and a source region doped with impurities of a first conductivity type separated by a channel doped with impurities of a second conductivity type where the source and drain regions are located in a vertical orientation. Hshieh also appears to teach a substrate with a conductivity type the same as that of the source and drain regions. Hshieh also appears to teach a single pocket formed in the drain region doped with impurities of the first conductivity type. For example, Hshieh states:

> The processing steps for manufacturing the improved p-channel power MOSFET device 200 with low threshold voltage according to the present invention are illustrated in FIGS. 6A to 6D. As shown in FIG. 6A, the processing steps begins by first growing a P^- epitaxial layer 210 with a resistivity ranging from 0.1 to 2.0 ohm-cm on top of a P^+ substrate 205. (Hshieh, column 5, lines 28-34)

> Thus, the present invention further discloses a MOSFET device 200 formed in a semiconductor chip 205 with a top surface and a bottom surface. The device 200 includes a drain region 210, doped with impurities of a first conductivity type, formed in the semiconductor chip 205 near the bottom surface. The MOSFET device 200 further includes a vertical pn-junction region includes a lower-outer body region [230], doped with impurities of a second conductivity type, formed on top of the drain region 210. The pn-junction region further includes a source region 250, doped with impurities of the first conductivity type, formed on top of the lower-outer body region [230] wherein the lower-outer body region [230] forming a channel region extending from the source region 250 to the drain region 210 near the top surface. The MOSFET device 200 further includes a gate 225 formed on top of the channel region on the top surface, the gate 225 includes a thin insulative bottom layer 220 for insulating from the channel region. The gate 225 is provided for applying a voltage thereon for controlling a current flowing from the source region 250 to the drain region 205 via the channel region. The MOSFET device 200 further includes a threshold reduction zone 240 near the top surface close to a boundary between the source region 250 and the lower-outer body region 235 wherein the threshold reduction zone 240 is selectively implanted with impurities of a conductivity type same as that of the source region 250 whereby a threshold voltage for the device 200 is reduced. (Hshieh, column 6, line 43 through column 7, line 2)

Hshieh does not appear to teach or suggest the presence of a first and a second pocket. Hshieh also does not appear to teach or suggest a source and drain region with a conductivity of a type different from that of the substrate. Applicant respectfully submits that the Examiner has mischaracterized FIG. 6D. As cited above, Hshieh describes a source and drain region as denoted by 250 and 210 respectively as opposed to the Examiner's notations of 265. Further, Hshieh describes the region denoted by 230 (incorrectly cited in the specification as 235) as the channel region rather than a second pocket as suggested by the Examiner. In addition, Hshieh does not appear to teach or suggest any required or preferred length of the doped sections.

As cited above, Applicant's claims 9 and 16 are directed to a combination of features including "a semiconductor substrate having a predetermined concentration, Ns, of a dopant of a first conductivity type", "a source region and a drain region doped with a dopant of a second conductivity type", "first pockets located adjacent to each of the junctions, wherein the pockets have a predetermined length, Lp, wherein the first pockets are doped with a dopant of the first

conductivity type with a dopant concentration, Np, which locally increases a net concentration in the substrate above Ns", and "second pockets located adjacent to each of the junctions and stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, and wherein the second pockets are doped with a dopant of the second conductivity type with a dopant concentration, Nn, such that Nn is less than Np, which locally decreases a net concentration without changing a conductivity type, and wherein Nn is less than Ns". Applicant submits that at least these features, in combination with the other features of the claims, are not taught or suggested by Hshieh. Applicant respectfully requests removal of the rejections of claims 9 and 16 and the claims dependent thereon.

The Examiner states: "With respect to claims 10, 12, Hshieh discloses that the second pockets (230) comprise a plurality of elementary pockets stacked against each other (fig. 6D)."

The Examiner further states: "With respect to claim 17, Hshieh discloses that the second pockets (230) comprise a plurality of elementary pockets stacked against each other (fig. 6D)."

Claim 10 describes features including: "wherein the second pockets comprise a plurality of elementary pockets stacked against each other." Claim 12 describes features including: "wherein the second pockets comprise a plurality of elementary pockets stacked against each other, and wherein the plurality of elementary pockets comprises three elementary pockets." Claim 17 describes features including: "wherein implanting in the channel region comprises a series of successive implanting steps such that the second pockets comprise a plurality of elementary pockets."

As noted above, Hshieh does not appear to teach or suggest a second pocket. Hshieh defines the channel region in column 6, lines 54-55, "wherein the lower-outer body region [230] forming a channel region extending from the source region 250 to the drain region 210 near the top surface." Accordingly, Hshieh appears to teach that the region denoted by 230 is a channel region and not a second pocket. In addition, Hshieh does not appear to teach or suggest that the channel region varies in dopant concentration. Hshieh, therefore, does not appear to teach or

suggest the presence of "a plurality of elementary pockets stacked against each other." Applicant respectfully requests removal of the rejections of claims 10, 12, and 17.

The Examiner states: "With respect to claim 14, Hshieh discloses that the first conductivity type comprises P-type conductivity. With respect to claim 15, Hshieh discloses that the second conductivity type comprises n-type conductivity."

The Examiner further states: "With respect to claim 26, Hshieh discloses that the first conductivity type comprises P-type conductivity. With respect to claim 27, Hshieh discloses that the second conductivity type comprises n-type conductivity."

Claims 14 and 26 describe features including: "wherein the first conductivity type comprises p-type conductivity." Claims 15 and 27 describe features including: "wherein the second conductivity type comprises n-type conductivity."

Applicant's claims 9 and 16 recite, in part: "a source region and a drain region doped with a dopant of a second conductivity type." Accordingly, the source and drain regions as described in claims 15 and 27 are of n-type conductivity. Hshieh, however, appears to teach that the source and drain regions are of p-type conductivity. For example, Hshieh states:

> As shown in FIG. 6A, the processing steps begins by first growing a P^- epitaxial layer 210 with a resistivity ranging from 0.1 to 2.0 ohm-cm on top of a P^+ substrate 205. (Hshieh, column 5, lines 31-34)
>
> Referring to FIG. 6C, a p+ block mask 245 is applied to carry out a p^+ implant to form the p^+ region 250. (Hshieh, column 5, lines 62-63)
>
> The device 200 includes a drain region 210, ...(Hshieh, column 6, lines 45-46)
>
> The pn-junction region further includes a source region 250,...(Hshieh, column 6, lines 51-52)

Applicant submits that Hshieh appears to teach a conductivity type configuration opposite that of Applicant. Applicant respectfully requests removal of the rejections of claims 14, 15, 26, and 27.

The Examiner states:

With respect to claim 28, Hshieh (figs. 6A-6D, cols. 5-6) discloses a semiconductor device, comprising;

a semiconductor substrate (210) having a concentration, Ns, of a dopant of a first conductivity type;

a source region (265) and a drain region (265) doped with a dopant of a second conductivity type;

junctions that define a channel region of a length, L_N, in the substrate, wherein the junctions are defined by the source region and the drain region;

first pockets (250) located adjacent to each of the junctions, wherein the first pockets have a length, Lp, and wherein the first pockets are doped with a dopant of the first conductivity type with a dopant concentration, N_P;

second pockets (230) stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, wherein the second pockets are doped with a dopant of the second conductivity type with a dopant concentration, Nn, such that Nn is less than Np; and

wherein an overall length of the first pockets and the second pockets is less than the length, LN, of the channel region (fig. 6D).

Claim 28 describes a combination of features including:

a semiconductor substrate having a concentration, Ns, of a dopant of a first conductivity type;

a source region and a drain region doped with a dopant of a second conductivity type;

junctions that define a channel region of a length, L_N, in the substrate, wherein the junctions are defined by the source region and the drain region;

first pockets located adjacent to each of the junctions, wherein the first pockets have a length, Lp, and wherein the first pockets are doped with a dopant of the first conductivity type with a dopant concentration, Np;

second pockets stacked against each of the first pockets, wherein the second pockets have a length, Ln, such that Ln is greater than Lp, wherein the second pockets are doped with a dopant of the second conductivity type with a dopant concentration, Nn, such that Nn is less than Np; and

wherein an overall length of the first pockets and the second pockets is less than the length, L_N, of the channel region.

Applicant submits that at least for the reasons provided above, the features of claim 28 are not taught or suggested by Hshieh. Applicant respectfully requests removal of the rejection of claim 28.

D. Summary

Based on the above, Applicant submits that all claims are in condition for allowance. Favorable reconsideration is respectfully requested.

Applicant respectfully requests a one-month extension of time to respond to the Office Action dated February 12, 2003. A Fee Authorization is enclosed to cover the one-month extension of time. If any additional extension of time is required, Applicant hereby requests the appropriate extension of time. If any additional fees are required, or if fees have been overpaid, please charge or credit those fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 50-1505/5310-03900/EBM.

Respectfully submitted,

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